We Claim:

1. A circuit configuration, comprising:

a programmable link being programmable with regard to its state of conduction by an energy pulse;

a drive circuit having an input side with an activation input and an output providing the energy pulse, said drive circuit coupled to said programmable link in a manner dependent on signals present on said input side; and

a shift register having at least one register cell for storing an activation signal, said shift register coupled to said activation input of said drive circuit for activating said drive circuit in a manner dependent on a memory content of said register cell.

2. The circuit configuration according to claim 1,

wherein said input side has a data input; and

further comprising a volatile memory cell coupled to said data input of said drive circuit for communicating a data signal for permanently altering the state of conduction of said programmable link in a manner dependent on a memory content of said volatile memory cell.

3. The circuit configuration according to claim 2, wherein said programmable link is an antifuse which, upon application of the energy pulse, permanently changes from a non-conducting state to a conducting state.

4. The circuit configuration according to claim 2, wherein:

said drive circuit contains a blowing transistor having a control input coupled to said activation input and to said data input and a controlled path with a first terminal for receiving a blowing voltage and a second terminal coupled to said programmable link; and

said blowing transistor, in a manner dependent on signals present at said activation and data inputs, connects said first terminal of said controlled path, at which the blowing voltage is received, with a low impedance to said second terminal of said controlled path, which is coupled to said programmable link.

5. The circuit configuration according to claim 4, wherein said drive circuit has a circuit for level boosting coupled to said blowing transistor.

6. The circuit configuration according to claim 2, wherein said drive circuit has an AND logic circuit, which combines said activation and data inputs with one another in an AND logic, said AND logic circuit having an output side coupled to said programmable link for driving said programmable link.

7. The circuit configuration according to claim 1, wherein:

said register cell has an input and an output; and

said shift register has an input, an output, a first switch receiving and controlled by a first clock signal for coupling said input of said shift register to said input of said register cell, and a second switch receiving and controlled by a second clock signal for coupling said output of said register cell to said output of said shift register.

8. The circuit configuration according to claim 1, wherein the circuit configuration is constructed using CMOS circuit technology.

9. A memory chip, comprising:

a programmable link being programmable with regard to its state of conduction by an energy pulse;

a drive circuit having an input side with an activation input and an output providing the energy pulse, said drive circuit coupled to said programmable link in a manner dependent on signals present on said input side; and

a shift register having at least one register cell for storing an activation signal, said shift register coupled to said activation input of said drive circuit for activating said drive circuit in a manner dependent on a memory content of said register cell.